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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

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149	Aiken, A., et al., "Optimal Loop Parallelization", <u>SIGPLAN Notices</u> , Vol. 23(7), ACM Press, 308-317, (July 1988)
	Dehnert, J.C., et al., "Overlapped Loop Support in the Cydra 5", <u>ASPLOS-III Proceedings Third International Conference on Architectural Support for Programming Languages and Operating Systems</u> , 26-38, (Apr. 1989)
	Ebcioğlu, K., "A Compilation Technique for Software Pipelining of Loops with Conditional Jumps (Preliminary Version)", <u>Proceedings of the 20th Annual Workshop on Microprogramming and Microarchitecture</u> , 69-79, (Dec. 1987)
	Rau, B.R., "Iterative Modulo Scheduling", <u>International Journal of Parallel Programming</u> 24(1), 3-64, (Feb. 1996)
	Rau, B.R., et al., "Code Generation Schema for Modulo Scheduled Loops", <u>SIG MICRO Newsletter</u> 23(1)(2), 158-159, (Dec. 1992)
129	Rau, B.R., et al., "Some Scheduling Techniques and an Easily Schedulable Horizontal Architecture for High Performance Scientific Computing", <u>14th Annual Microprogramming Workshop</u> , 183-198, (Oct. 1981)

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*Substitute Disclosure Statement Form (PTO-1449)

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